A

TECHNICAL DESCRIPTION

OF A

SIGNAL PROCESSOR CONTROLLER

Submitted to

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Electromagnetic Systems Division

BY

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.0 MACHINE ARCHITECTURE

.1 Introduction

The Airborne Microprogrammable Processor, AMPP, presently under development at Control Data Corporation, is a re-packaged and improved version of the present MPP. The repackaged version uses essentially the same machine organization as the present MPP with circuitry designed for MIL-E-5400 applications and normal product improvement to assure low risk.

.2 AMPP Functional Description

A simplified block diagram of the AMPP is shown in Figure 1. The MICRO PROGRAM MEMORY contains up to 4096 64-bit words. This is sufficient local memory for all firmware requirements. These 64-bit words are referred to as MICRO COMMANDS and are read into the MICRO I REG at the normal rate of one each 150 nanoseconds. The 64-bit MICRO COMMANDS are broken up into a number of fields which control all operations in the AMPP. In a given MICRO COMMAND, fields exist for selection {through the MICRO CONTROLLER SELECTION GATES} of two 16-bit quantities to be placed on the A and B bus, an operation to be performed on the A and B bus data, and a destination for the result on the C bus. Simultaneously, other fields of the MICRO COMMAND word are used for testing internal and external status for selection requesting instruction and operand memory {RAM} and for providing literal data.

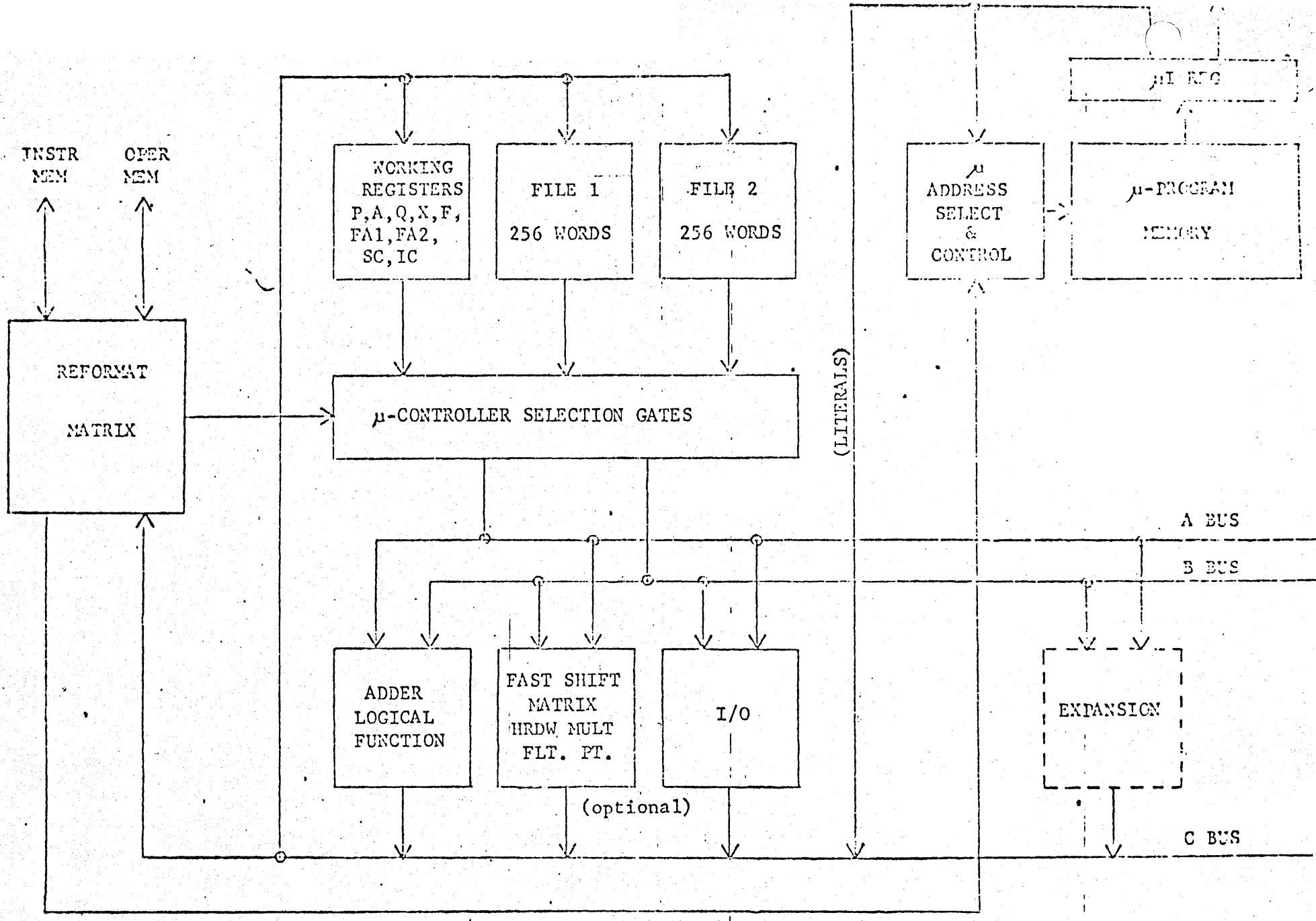


FIGURE 1. AMPP BLOCK DIAGRAM

AMPP Random Access Memory (RAM) Organization

The RAM is organized as a contiguous block of 4096 16-bit words for the Receiver Controller and 2,048 16-bit words for the Transmitter Controller. Each memory is physically located on a single pluggable module which can contain a maximum 8,192 16-bit words.

Expansion for the Transmitter Controller memory may be implemented on the single module.

Full expansion of the Receiver Controller memory to 12,288 16-bit words will require an additional modules.

Individual access ports for each 2K of memory will be provided.

.4 AMPP Interrupt Structure

The interrupt structure of the AMPP is firmware controlled. Priority is assigned according to the following structure:

1. Power Failure Auto Restart
2. Internal AMPP Fault
3. Real Time Clock and I/O

.5 Direct Memory Access Channels

The AMPP as configured for either the Transmitter Controller or the Receiver Controller will provide Direct Memory Access

(DMA) channels to the data memory (RAM).

Data may be written into the AMPP data memory by an external source which provides a memory address, a Write Request, and the data word.

The AMPP will respond with a Resume signal indicating that data has been stored.

Data may be read out of the AMPP data memory by an external device which provides a memory address, and a Read Request.

The AMPP will respond by placing the data word on the lines and raising the Resume line.

The External device will acknowledge the data by dropping its Read Request.

I.6 Test Control Panel Interface

Each controller will have in addition to the two Direct Memory Access Channels, an interface to a test control panel. This interface will be compatible with an RS-232-C communications device. The Test Control Panel interface will be located on the I/O card.

I.7 Dead Start Facility

Each controller will include a Dead Start capability implimented in micro programmable ROM. Programming shall be

loaded via either the Test Control Panel Interface or the DMA interface from the medium speed digital computer.

.8 AMPP Options

As shown on the block diagram a number of logic functions options exist in the AMPP architecture. These options of:

1.) High Speed Shift Matrix

2.) Floating Point Option

3.) File 2 (256 16-bit registers)

The High Speed Shift Matrix and the Floating Point Option are discussed in Section 2.4 of this proposal. The 256 register File 2 option is used primarily for emulation of other processors, and as such, has not been considered for this application.

2.0 FIRMWARE ARCHITECTURE

2.1 Micro Memory Description

The micro memory contains up to 4096 64-bit words. In the final package configuration of the AMPP, this memory is constructed of read-only integrated circuits (ROM) and is partitioned on one pluggable card. During the initial phases of software/firmware checkout and flight testing, however, it will be advantageous to make use of a read/write micro memory. After all requirements have been firmed and the software/firmware has been checked, the read/write micromemory will be replaced by the final ROM card. Since the read/write memory consumes

more power and occupies more space than the final ROM micro memory, the read/write memory will be packaged in a separate enclosure as shown in Figure 2 which will not be required in the final equipment. The read/write micro memory will be constructed of random access integrated circuits (RAM), packaged with a separate power supply in a 1/2 ATR enclosure, and designed to meet flight environments.

2.2 Memory Overlap/Interleaving

The architecture in the AMPP is designed to allow either simultaneous access of instruction and operand from independent memories or sequential access from one memory. The memory may be organized to operate as a single large memory or two smaller independently accessed memories. While the two-memory system provides faster execution rates, it also consumes more power. A single memory organization, therefore, will be used to conserve power. With this organization, a certain degree of overlap still exists in the microprogramming. That is, given fields of a micro command are used to request a memory reference before the data are actually required. The reformat matrix in the AMPP actually fetches the word from memory and retains the information until interrogated by another micro command. The latter micro command is delayed only if a resume has not been received from memory. Both instruction and operand look-ahead and retention are provided in the reformat matrix.

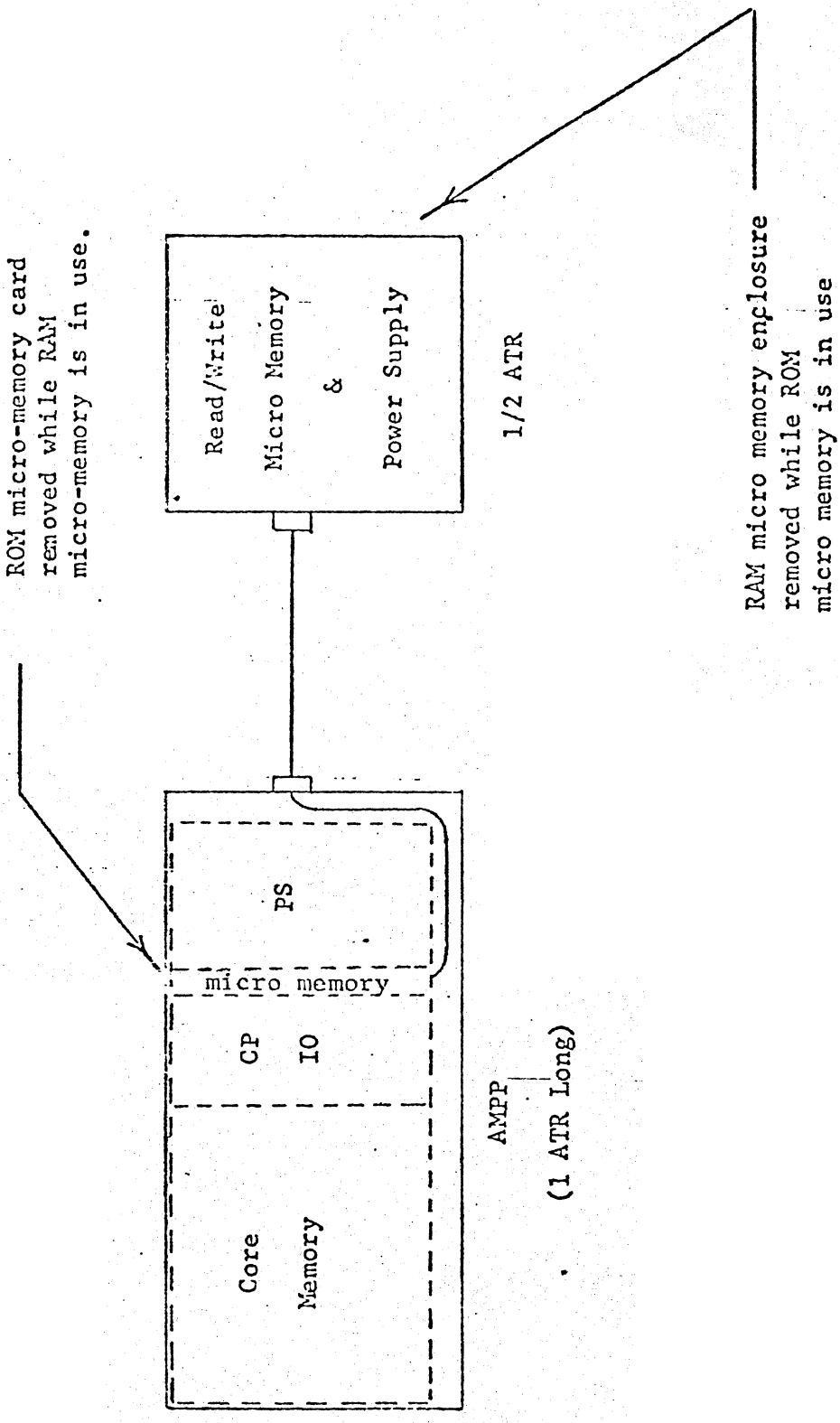


FIGURE 2

INTERIM PACKAGED READ/WRITE MICRO MEMORY

.3 Reformat Matrix

In addition to providing instruction and operand look-ahead and retention, the reformat matrix is used to adapt the common arithmetic section used in all AMPP's to the particular instruction format used in the machine it is emulating. That is, all machines for which the AMPP is intended to emulate do not utilize the same instruction format for operation code field, index field, file designator fields, base address fields, etc. - or even the same number of bits for that matter. The reformat matrix simply regroups or positions the bits for the common arithmetic section. It is interrogated by, and under control of the micro program. The reformat matrix is partitioned on a single pluggable card which is tailored for a particular machine.

.4 Floating Point Speeds

The basic AMPP (without options) can be programmed with firmware to execute any particular floating point package. for certain floating point word formats, a considerable amount of bit shuffling is required. When the program relies heavily upon floating point operations, a considerable improvement in speed is obtained by one or more of the options provided.

As shown in Figure 1, the A and B bus feed optional logic units. A 3-bit field (F) in each MICRO-COMMAND specifies the function

or logic unit to be used and an 8-bit sub-function field specifies the operation to be performed. The results are placed on the tri-state C bus, and directed to the destination register specified by a 4-bit D field in the MICRO COMMAND.

One of the optional logic units is the Floating Point Function. This unit requires only a small amount of hardware (approximately 1/6 of a pluggable card in the AMPP) and provides a number of functions such as reformatting of data on the A and B bus, binary point alignment count generation, normalization count generation, and overflow/underflow check. The first function removes the characteristic and closes up the mantissa with its sign bit. The second function generates the proper absolute magnitude characteristic difference. The third function generates the proper shift count required to normalize a result.

Another optional logic unit is the High Speed Shift Matrix. This unit will shift the quantities placed on the A and B bus by the count specified in the SC register in one MICRO COMMAND step. The unit has many sub-functions such as left or right shifting, end off or sign extended, single or double length, byte and half word operations, bit inversion, circular, etc. which make it useful for emulation of other instructions besides floating point. It requires more hardware than the Floating Point Function (approximately 1/2 card in the AMPP).

3.0 CONTROLLER PERFORMANCE

3.1 General

The AMPP configured as the Signal Processor Controller will operate exclusively out of the high speed micro memory. This method of operation provides for a very efficient utilization of the AMPP architecture and an instruction execution rate in excess of 2,000,000 instructions per second.

3.1.1 Processing Speed

Using the instruction mix provided in Rayteon Specification 574017, the AMPP, using micro program control was evaluated for processing speed. The results of this evaluation are as follows:

INSTRUCTION	RATES	INSTRUCTION TIME (MICROSECONDS)	PRODUCT
Load (From Memory)	21%	.604	.1268
Store (To Memory)	24%	.436	.1046
Add/Subtract	9%	.660	.0594
Shift	10%	.600	.0600
Test & Branch	30%	.240	.0720
And,Or,Compliment	5%	.604	.0302
I-O Control	1%	1.000	.0100
	100%		.4630

INSTRUCTION EXECUTION SPEED 2,159,827 Inst/sec.

3.1.2 Interrupt Processing

3.2.1 General

Hardware interrupts are sampled during the instruction fetch portion of the emulation loop or at the completion of a pipeline segment in the application firmware. The maximum latency time between occurence and sampling of an interrupt is 100 us. Upon sampling, all interrupts are classified and processed in accordance with the present interrupt mask and the following priority structure:

Class	1	Power Failure Auto Restart
	2	Internal MPP Fault
	3	Real Time Clock, I/O Interrupts

3.2.2 Power Failure/Auto Restart

When the AMPP Power Supply detects a power failure condition an interrupt is initiated at least 500 usec before shutdown. Upon detection of this interrupt, the firmware saves the internal registers and status in core memory and sets an interrupt condition for software detection.

Upon resumption of a stable power condition or initial startup the AMPP Master Clear Sequence is entered, the internal registers are reloaded from memory, the panel mounted load switch is tested and if set the firmware bootstrap executed.

1.2.3 I/O Interrupts

Hardware I/O interrupts are classified as to whether they are associated with buffered I/O operations, programmed I/O, or the DMA channel. The latter two types cause Busy to be cleared and a software interrupt to be initiated. In the case of buffered I/O the word count is decremented and tested for zero. If zero, a software interrupt is established in the usual manner. If non-zero, the buffer address is incremented and the next word transfer initiated without interruption of the software.

4.0 PACKAGING

4.1 Physical Description

Control Data proposes to package both the Transmitter Controller and the Receiver Controller in a single enclosure occupying approximately 0.875 cu. ft. (1510 cubic inches) shown in Figure 3. The packaging concept consists of a modular philosophy made up of a power supply, four (4) logic modules and one (1) RAM Module per AMPP controller. RAM modules can contain a maximum of 8K by 16-bit as presently configured. Expansion of the RAM for individual controllers will be implimented utilizing spare module locations. This modular concept enhances maintainability, handling, expansion, and logistics. Table 1 presents a summary of physical and cooling characteristics.

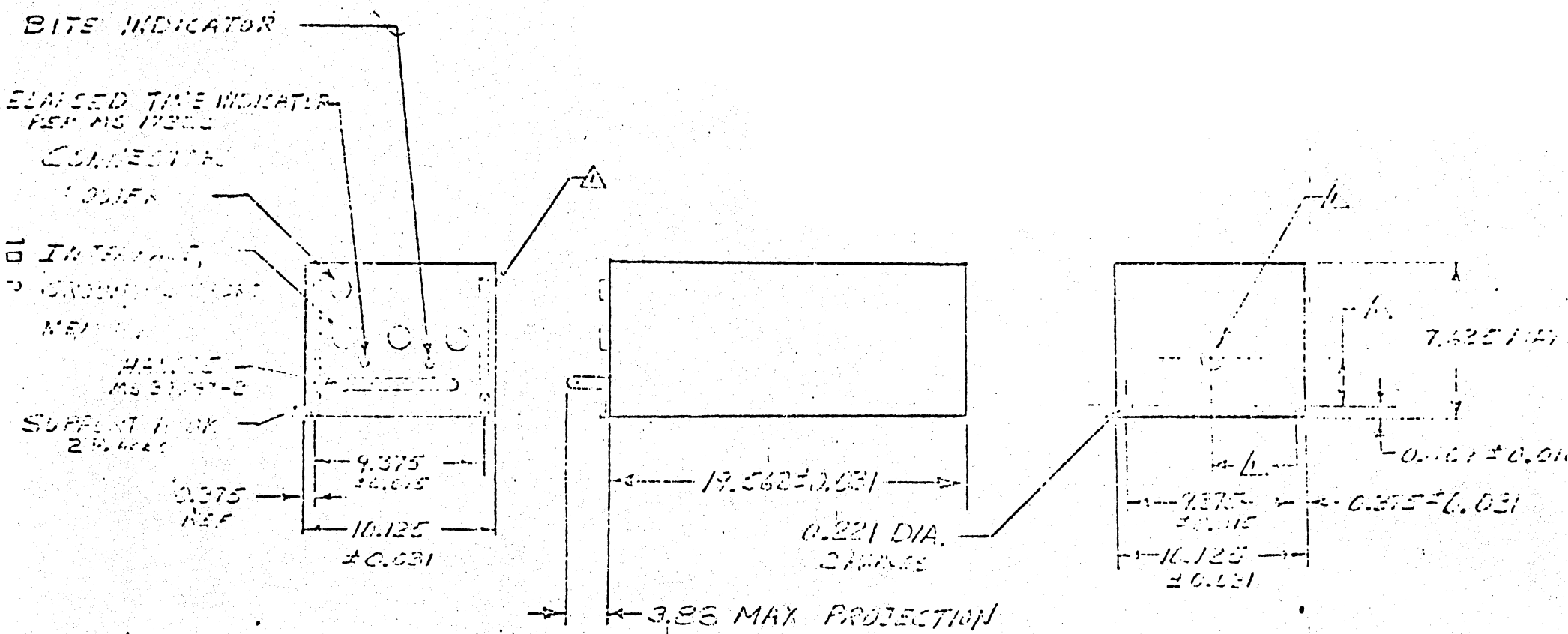
TABLE 1. PHYSICAL CHARACTERISTICS

Volume	0.875	Cubic Feet
Height	7.625	Inches
Width	10.125	Inches
Length	19.562	Inches
Weight	40	Pounds
Input Power	500	Watts

Cooling

Air at 55°C	1.5 pounds/minute
Air at 25°C	0.88 pounds/minute
Pressure Drop	2.0 inches of H_2O maximum at 70°F inlet air temperature, sea level pressure, including inlet header loss, core loss, and exit loss.

OUTLINE DRAWING



△ LOCATION DIMENSIONS AND SIZES FOR AIR TO BE DETERMINED.

2. ENCLOSURE DIMENSIONING PER MS 91403-BID2.

FIG 3

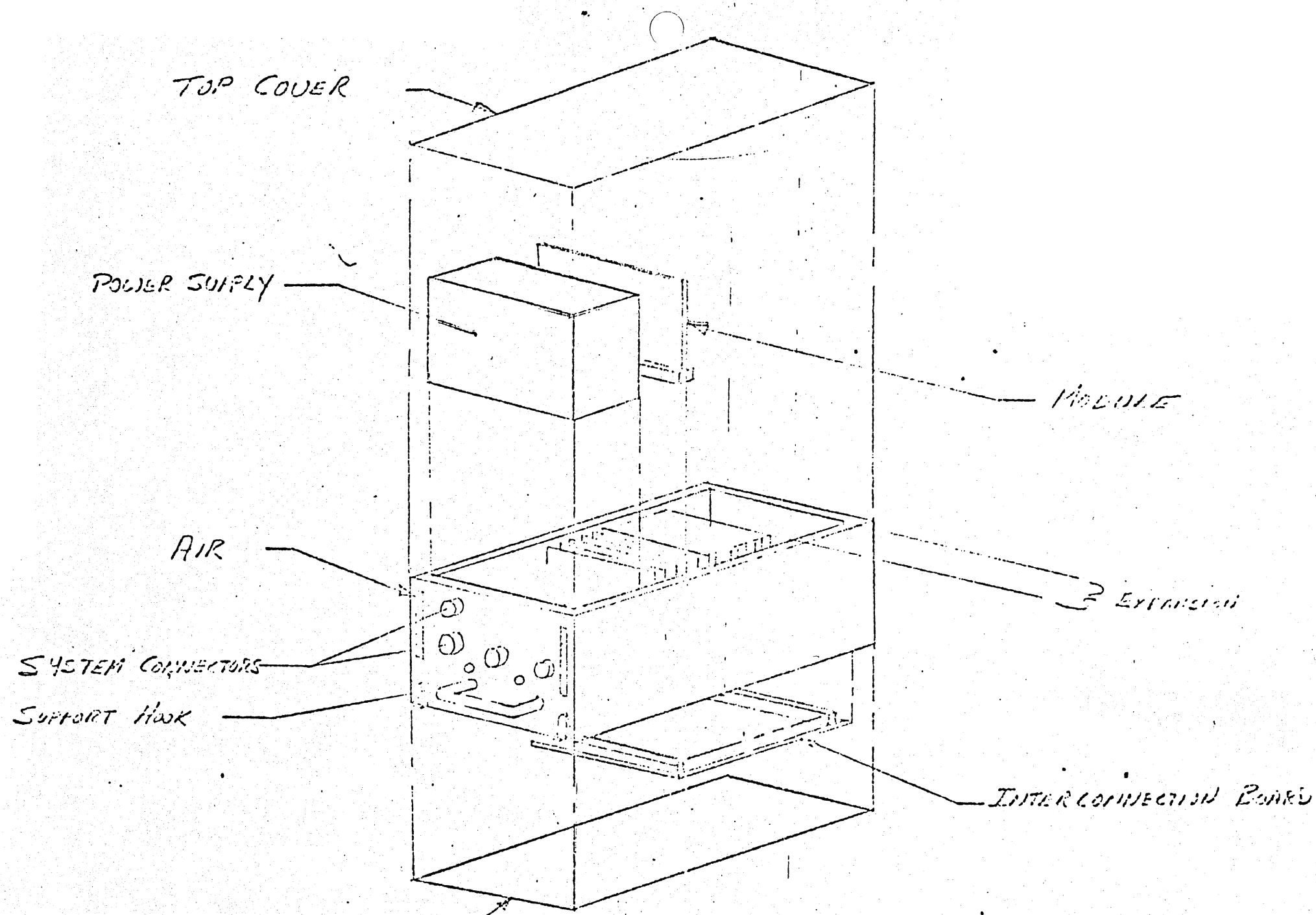


FIG 4 AMPP MODULAR CONCEPT

The enclosure is a standard full ATR size consisting of an aluminum chassis into which an interconnection board and plenum assembly are mounted. System interface connectors are per MIL-C-81511 (e.g. power receptacle M81511/23ED02P1) and mount to the front panel of the enclosure and are hard wired to the interconnection board assembly with the capability of being removed as a complete assembly. The top and bottom panels can be easily removed providing access to MPP modules, memory modules, power supply and interconnection board assembly.

The modules consist of individual heat exchangers laminated between two circuit boards with printed circuit connectors conforming to MIL-C-55302 for connection to the interconnection board. The modules plug into the interconnection board and air plenum assembly. Components mounted on the circuit boards are conduction-cooled by conducting the heat through the circuit board via plated-through holes to the heat exchanger which is convection cooled by air flowing from the supply plenum to the exhaust plenum. This cooling design represents a parallel flow cooling system. Conduction cooling is desirable since it isolates the modules and components from contaminants such as fungus, sand, dust, moisture and salt which could be present in the cooling air. The overall design is compatible with MIL-E-5400, Class 1AX.

5.0 SOFTWARE PACKAGE

The software package to be provided with the AMPP Signal Processor Controllers consist of that software which is required to program, operate and maintain a micro-programmable processor in which all instructions are executed from micro memory. Since this is the case, several of the software packages required by SOW:MAS:73:042, paragraph 3.1.2 are not applicable. These are:

1. Self Assembler
2. Relocatable Loader/Verifier
3. De-Bug Program

Software which is applicable to the AMPP Signal Processor Controllers are:

1. A MICRO COMMAND translator which translates symbolic source program commands into object machine commands.
2. Hardware Diagnostic Software which detects processor faults via software and firmware.
3. Interface Handlers for Signal Processor Controller peripherals.

5.1 Hardware Diagnostic Package

5.1.1 Fault Detection

Hardware faults are detected through off-line and on-line fault detection firmware and software.

Off-line fault detection software requires a system dedicated for testing and provides complete fault detection. Manual operations by an operator are required to initiate, observe, and supplement the tests. The contents of memory are destroyed, and all I/O operations are suspended when the off-line fault detection is in execution. The off-line fault detection tests are used at any time a complete system verification is required.

On-line fault detection consists of automatic portions of the off-line tests. The on-line fault detection tests operate on a non-conflicting basis with the operational software. They are continuously executed on a low-priority basis to provide system confidence. Operating personnel are notified if any malfunctions are detected.

The off-line fault detection tests are made up of resident firmware {micro commands} tests for testing processor logic. All memory and I/O interface logic are tested with software. This software is loadable from magnetic tape.

The on-line fault detection tests are made up of the same basic resident firmware test. The memory and I/O interfaces are tested with resident software.

Fault Isolation diagnostic test routines are off-line initiated when system or subunit malfunctions are suspected. Malfunctions are detected through visual observations by operating personnel or by on-line fault detection diagnostics.

5.1.2 Fault Isolation Philosophy

The diagnostic test program and manual procedures are referred to as Diagnostic Software. The Diagnostic Software is a tool which along with logic diagrams, wire lists and standard test equipment, enable a trained computer technician to correct computer malfunctions.

The tests are largely automatic, i.e., do not require operator intervention. Any failure which prohibits normal program loading and program execution necessitates manual fault isolation. No-load failures can be in the Processor, Memory or Magnetic Tape. Fault isolation of No-load failures is accomplished by manually initiating and observing the results of tests in the Diagnostic Software.

Failure signatures are identified through failure codes and are observed by the computer technician at the maintenance panel. The computer technician will reference the Computer Program Operator's Manual and will identify the failing signal. The cards on which the failing signal occurs are also identified in the same manual. The computer technician

has the option of attempting further isolation with standard test equipment and troubleshooting techniques, or he can change each card identified in the Diagnostic Users' Manual.

5.1.3 Extent of Testing

All logic is tested with the Off-Line Diagnostic Software. Self-test capability has been incorporated into the processor.

5.2 Micro Command Translator

The MICRO-73 Command Translator for the Control Data Airborne Microprogrammable Processor (AMPP) provides the mnemonic language necessary for the programmer to write microprograms. MICRO-73 translates symbolic source program commands into object machine commands and also provides a listing of the translator results.

The base version of MICRO-73 is written for the CDC 3300 computer. This base version of MICRO-73 is written in Fortran with a minimum of machine language routines included, and thus is easily transferrable from one type of computer to another type of host computer. Currently, versions of MICRO-73 are planned for the CDC 6600 and IBM series 360-370 computers.

Input to MICRO-73 is in the form of cards or card images, containing symbolic AMPP program commands. The output is

is object code on cards, magnetic tape, or paper tape along with a printer listing of the microprogram with additional debugging diagnostics generated by the MICRO-73 Command Translator.

6.0 SUPPORT EQUIPMENT

6.1 Maintenance Panel

The maintenance panel developed for use with the Control Data 5600 Series of MPP's contains all of the controls and functions that are anticipated to be necessary for use in either hardware debug or as an operators console (See Table 2). It is suggested that this panel be examined functionally in light of the system maintainability requirements as well as the prototype development requirements. The maintenance panel with its functions will connect to the AMPP through a service connector on the AMPP front panel. This connector will not be used for any other purpose.

TABLE 2. MPP CONTROLS AND INDICATORS

Panel Nomenclature	Device	Function
DATA 0 to 15	Indicator lights	Displays current binary data as determined by positions of SELECT switch and pushbuttons.
DATA 0 to 15	Toggle switches	Specify input data or address. Up position = 1; down position = 0. When TRANSFER DATA switch is depressed, number set in DATA switches is transferred to register specified by SELECT switch and pushbuttons. When TRANSFER ADDRESS switch is depressed, number set in DATA switches is transferred to address register specified by ADDRESS SELECT switch.
DDRESS 0 to 15	Indicator lights	Indicate address being referenced. Address displayed is specified by ADDRESS SELECT switch. Indicators at bit positions 0, 1, 2, and 3 indicate state of test bit (TB), full word (FW), half word (HW), character (CHAR) signals. The FW, HW, and CHAR indicators comprise a character counter that indicates which two 8-bit characters are addressed (not applicable for MPPs containing dead start option).
ADDRESS SELECT	Rotary switch	Specifies address for display on ADDRESS indicators and for transfer address or advance address operations. • MEM: main memory • N: N register • K: K register • MM: micromemory address register

TABLE 2. MPP CONTROLS AND INDICATORS (Cont.)

Panel Nomenclature	Device	Function
ADDRESS SELECT (Cont.)	Rotary switch	Contents of N is displayed on DATA indicators 0-7. When MEM is specified, address of last main memory read or write operation is displayed on ADDRESS indicators (only for MPPs with breakpoint option). Contents of K and MM address register is displayed on ADDRESS indicators.
ADVANCE	Toggle switch	Specifies that MM address will be advanced by a character (CHAR), by an MM page (PAGE), or by one MM instruction (ONE) when ADVANCE ADDRESS is depressed. (CHAR position not used in MPPs with dead start option.)
ADVANCE ADDRESS	Pushbutton	Causes address specified by ADDRESS SELECT to advance by one when depressed, for N and K. Causes address to advance by one character, one page, or one instruction for MM. MEM can not be advanced by depressing ADVANCE ADDRESS pushbutton.
TRANSFER ADDRESS	Pushbutton	Transfers quantity set into DATA switches to N, K, or MM, as specified by ADDRESS SELECT switch. TRANSFER ADDRESS has no effect when ADDRESS SELECT specifies MEM.
TRANSFER DATA	Pushbutton	Transfers quantity set into DATA switches to destination specified by SELECT switch and pushbuttons, if destination can accept data from maintenance panel (refer to SELECT).
SELECT	Toggle switch and pushbuttons	
• $\overline{\text{MIRU}}$, $\overline{\text{MIRL}}$		Specifies that complement of quantity set into DATA switches is to be transferred to MIR upper portion (bits 0-15) or to MIR lower portion (bits 16-31) when TRANSFER DATA is depressed. Contents of MIR is not displayed on DATA indicators.

TABLE 2. MPP CONTROLS AND INDICATORS (Cont.)

Panel Nomenclature	Device	Function
o SM1, SM2, MMU		Specifies status/mode register 1 (SM1), SM2, or upper half of micromemory location (MMU) for display or data transfer. NOTE Data can be transferred to MM only if MPP has a read/write MM and MM ENABLES/WRITE switch is in up position.
o M1, M2, MML		Specifies mask register 1 (M1), M2, or lower half of MM location (MML) for display or data transfer.
o F2, F1		Specifies register file 2 (F2) or F1 for display or data transfer.
o X, F		Specifies X or F register for display or data transfer.
o I, X*, BG		Specifies I or X* register for display or data transfer. Specifies bit generator (BG) for display. Output of BG controlled by micro-instruction, or by lower five bits of N register if flag 3 of SM1 is set.
o A, A*, Q		Specifies A, A*, or Q register for display or data transfer.
o P, Q', N/RTJ		Specifies P or Q' register for display or data transfer. When N/RTJ is selected, contents of N is displayed on DATA indicators 0-7 and contents of RTJ is displayed on DATA indicators 8-15. N can be loaded by transfer address operation if ADDRESS SELECT is set to N. RTJ is alterable only by execution of microinstruction.
PE	Indicator light	Indicates a main memory parity error (PE) when lighted.
PROT	Indicator light	Indicates MPP is in protect mode (systems containing optional program protect logic).

TABLE 2. MPP CONTROLS AND INDICATORS (Cont.)

Panel Nomenclature	Device	Function
DS	Indicator light	Indicates MPP is in dead start (DS) mode.
SEL JUMP	Toggle switch	In up position, interpreted by firmware to indicate selective jump is required.
SEL STOP	Toggle switch	In up position, interpreted by firmware to indicate selective stop is required.
LOAD MM/OFF/MEM	Toggle switch	Used for selecting micromemory (MM) or main memory (MEM) for loading. DS indicator lights when set to LOAD MM. Loading starts when START switch is depressed.
PROTECT/OFF/ MICRO REPEAT	Toggle switch	Enables optional protect system when set to PROTECT. When set to MICRO REPEAT, instruction currently in MIR register is repeated continuously when START is depressed.
STEP INST/OFF/ MICRO	Toggle switch	Specifies that each time START is depressed, program execution will halt after executing one software instruction (INST) or after executing one microinstruction (MICRO).
ENTER/OFF/SWEEP	Toggle switch	Switch whose position can be sensed by microinstructions.
PANEL LOCKOUT	Toggle switch	In up position, disables main function switches except MAIN POWER. SELECT and ADDRESS SELECT still operable for display purposes.
MAIN POWER ON/OFF	Toggle switch	Controls AC power input to processor enclosure.

TABLE 2. MPP CONTROLS AND INDICATORS (Cont.)

Panel Nomenclature	Device	Function
MM ENABLES	Toggle switches	
o WRITE		In up position, enables writing into read/write micromemory through DATA and TRANSFER DATA switches.
o ADDRESS HOLD		In up position, prevents MIR from being cleared when MASTER CLEAR depressed. Allows microprogram to be started at location specified by MM address register.
START	Pushbutton	Starts program execution.
RUN	Indicator light	Indicates processor is running when lighted.
STOP	Pushbutton	Stops program execution when next micro-instruction containing a halt code is executed.
MASTER CLEAR	Pushbutton	Clears MPP logic circuits.
BREAKPOINT MM/ OFF/MEM	Toggle switch	Specifies that processor is to halt at micromemory address (MM) or at main memory address (MEM), in systems containing breakpoint option.
Breakpoint	Thumbwheel switches	Specify hexadecimal address at which processor is to stop, if enabled by BREAKPOINT MM/OFF/MEM switch.